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ART UNIT	**PAPER NUMBER**
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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/721,606	Applicant(s) SUL ET AL.
	Examiner Chun-Kuan (Mike) Lee	Art Unit 2181

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 25 November 2003.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-25 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-25 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 25 November 2003 is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Supervisory

FRITZ FLEMING
PRIMARY EXAMINER
GROUP 2100
6/14/2006
AU 2181

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The disclosure is objected to because of the following informalities:

on page 8, lines 31, the Specification teaches that Fig. 10, ref. 96 is an OR-gate, but the Drawings shows that it is an XOR-gate. Examiner will assume that Fig. 10, ref. 96 is an XOR-gate for the current examination; and

on page 2, in 1^{st} and 2^{nd} paragraph, reference numbers associated with the compactor, the cyclic shift register, the number of scan chains and the XOR-gate appear to be to be different than the reference number utilized in Figure 2 of the Drawings. It appears that the compactor should have reference number 9, the cyclic shift register should have reference number 12, the number of scan chains should have reference number 10 and the XOR-gate should have reference number 11.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 1-3 and 5-17 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

3. Claim 6-7 recites the limitation "I/O pin" in claim 6, lines 4-5 and in claim 7, lines 3-4. There is insufficient antecedent basis for this limitation in the claim.

4. As per claims 1-3 and 5-17, applicant recited in each of the respective climes the claimed limitation utilizing the term “operable to,” wherein the term “operable to” is not a positive limitation, but rather a suggestion as to what the claimed limitation may be capable of. Examiner will assume, for each respective claims, that the stated functionality associated with “operable to” is considered as a potential capability rather than a positive limitation for the current examination.

5. As per claims 6-7, it appears unclear as to which “I/O pin” the applicant is referring to, as claims 6-7 is dependent on claims 1-2, wherein claim 2 recites the limitation “first I/O pin” and claim 1 recites the limitation “a plurality of pins,” therefore it appears unclear if the “I/O pin” is the “first I/O pin” or a different I/O pin. Examiner will assume “first I/O pin” for the current examination of claims 6-7.

6. As per claim 11, it appears the applicant repeated the claimed limitation “each I/O pin is operable to input scan test data during the test time.” Examiner will remove one of the repeated claimed limitation for the current examination.

7. As per claim 16, it appears unclear, base on the Drawings, Fig. 10, ref. 96, how the output of the linear feedback shift register is inputted into the OR-gate as the

Drawings show that the output of the linear feedback shift register is inputted into a XOR-gate. Examiner will assume that the claimed limitation is "XOR-gate" for the current examination.

Claim Rejections - 35 USC § 102

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

8. Claims 1 and 8-9 are rejected under 35 U.S.C. 102(a) as being anticipated by Applicant's Admitted Prior Art (AAPA).

9. As per claim 1, AAPA teaches an integrated circuit comprising:

a plurality of pins (Drawings, Fig. 1, ref. 2, 12); and

at least one scan path (Drawings, Fig. 1, ref. 9) per pin (input pin 2 of Fig. 1).

10. As per claim 8, AAPA teaches an integrated circuit comprising:

a first I/O pin (Drawings, Fig. 1, ref. 2) operable to receive input data during a test time (Specification, page 1, ll. 5-6); and

a second I/O pin (Drawings, Fig. 1, ref. 12) operable to provide output data during the test time (Specification, page 1, ll. 5-6).

11. As per claim 9, AAPA teaches an integrated circuit further comprising a first scan path (Drawings, Fig. 1, ref. 9) wherein:

the first I/O pin (Drawings, Fig. 1, ref. 2) is operable to input scan test data during the test time (Specification, page 1, ll. 5-8); and

the second I/O pin (Drawings, Fig. 1, ref. 12) is operable to output scan test data during the test time (Specification, page 1, ll. 5-8).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

12. Claims 2-7 and 10-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA in view of Chennupati (US Patent 6,833,728).

13. As per claim 2, AAPA teaches the integrated circuit comprising:

wherein a first I/O pin (Drawings, Fig. 1, ref. 2) is operable to input scan test data at a first test time (Specification, page 1, ll. 5-6); and

a second I/O pin (Drawings, Fig. 1, ref. 12) is operable to output scan test data at a second test time (Specification, page 1, ll. 5-6).

AAPA does not teach the integrated circuit comprising wherein the first I/O pin is operable to output scan data.

Chennupati teaches a system and a method comprising a single bi-directional pin (Fig. 1, ref. 152) is utilized for both inputting and outputting of data (col. 1, ll. 15-17 and col. 4, ll. 23-25).

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to include Chennupati's bi-directional pin into AAPA's first and second I/O pins. The resulting combination of the references teaches the integrated circuit further comprising the first I/O pin is operable to input scan data during the first time and to output scan data during the second time.

Therefore, it would have been obvious to combine Chennupati with AAPA for the benefit of reducing the number pins or allow additional pins to be used for other purposes (Chennupati, col. 5, ll. 34-37).

14. As per claim 3, AAPA and Chennupati teach all the limitations of claim 2 as discussed above, where Chennupati further teaches the integrated circuit comprising:

the first I/O pin (I/O pin couple to L0 of Fig. 2) is operable to input scan test data to a first scan path at the first test time (Chennupati, col. 5, ll. 38-44), wherein the WRITE0 data is received through L0 bus line;

a second I/O pin (I/O pin couple to L1 of Fig. 2) is operable to input scan test data to a second scan path at the first test time (Chennupati, col. 5, ll. 38-44), wherein the WRITE1 data is received through the L1 bus line;

the first I/O pin (I/O pin couple to L0 of Fig. 2) is operable to output scan test data from the second scan path at the second test time (Chennupati, col. 5, ll. 38-44), wherein the READ1 is to be outputted to the L0 bus line; and

the second I/O pin (I/O pin couple to L1 of Fig. 2) is operable to output scan test data from the first scan path at the second test time (Chennupati, col. 5, ll. 38-44), wherein the READ0 is to be outputted to the L1 bus line.

15. As per claim 4, AAPA and Chennupati teach all the limitations of claim 3 as discussed above, where Chennupati further teaches the integrated circuit comprising wherein the first scan path further comprises a series of scan paths (Chennupati, Fig. 2 and col. 5, ll. 38-44), wherein the first of the series of scan path is the path for the transferring of write data into the memory and the second of the series of scan path is the path for the outputting of the read data from the memory.

16. As per claim 5, AAPA and Chennupati teach all the limitations of claim 2 as discussed above, where Chennupati further teaches the integrated circuit further comprising:

a series of scan paths (Chennupati, Fig. 2 and col. 5, ll. 38-44), wherein the first of the series of scan path is the path for the transferring of write data into the memory and the second of the series of scan path is the path for the outputting of the read data from the memory, wherein:

the first I/O pin is operable to input scan test data to the series at a first test time (Chennupati, Fig. 2 and col. 5, ll. 38-44), as the write data is send through the L0 bus line to the first I/O pin of the memory; and

the first I/O pin is operable to output scan test data from the series at a second test time (Chennupati, Fig. 2 and col. 5, ll. 38-44), as the read data is outputted by the memory, to the L0 bus line, through the first I/O pin.

17. As per claim 6, AAPA and Chennupati teach all the limitations of claim 2 as discussed above, where Chennupati further teaches the integrated circuit further comprising functional circuitry (Chennupati, memory 204 of Fig. 2) wherein:

the scan path interacts with the functional circuitry (Chennupati, Fig. 2 and col. 5, ll. 38-44), wherein data are transferred to and from the memory through the scan path; and

the first I/O pin is operable to input scan test data (write data) at the first test time (Chennupati, Fig. 2 and col. 5, ll. 38-44), as the write data is send through the L0 bus line to the first I/O pin of the memory; and

the first I/O pin is operable to output scan test data (read data) at the second test time (Chennupati, Fig. 2 and col. 5, ll. 38-44), as the read data is outputted by the memory, to the L0 bus line, through the first I/O pin.

18. As per claim 7, AAPA and Chennupati teach all the limitations of claim 2 as discussed above, where Chennupati further teaches the integrated circuit further comprising functional circuitry (Chennupati, memory 204 of Fig. 2) wherein:

the first I/O pin is operable to input functional test data (write data) at the first test time (Chennupati, Fig. 2 and col. 5, ll. 38-44), as the write data is send through the L0 bus line to the first I/O pin of the memory; and

the first I/O pin is operable to output functional test data (read data) at a the second test time (Chennupati, Fig. 2 and col. 5, ll. 38-44), as the read data is outputted by the memory, to the L0 bus line, through the first I/O pin.

19. As per claim 10, AAPA teaches the integrated circuit further comprising a second scan path wherein:

the first I/O pin (Drawings, Fig. 1, ref. 2) is operable to input scan test data to the first scan path during the test time (Specification, page 1, ll. 5-8); and

the second I/O pin (Drawings, Fig. 1, ref. 12) is operable to output scan test from the first scan path data during the test time.

AAPA does not teach the integrated circuit comprising a second scan path wherein:

the output from the first scan path is input to the second scan path; and

the second I/O pin is operable to output scan test from the second scan path data during the test time.

Chennupati teaches a system and a method comprising data is inputted into a device (Fig. 2, ref. 150) through a INPUT2 data path and outputted from the device through the OUTPUT2 data path (Fig. 1, ref. 156), wherein the received INPUT2 data would have been processed by other components in the device to generated the OUTPUT2 data to be outputted (Fig. 1 and col. 4, ll. 27-29).

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to include Chennupati's input and output data path in the device into AAPA's integrated circuit. The resulting combination of the references teaches the integrated circuit further comprising the first I/O pin inputting data into the INPUT data path (first scan path), wherein the inputted data is processed by the plurality of components and the result of the processing is outputted onto the OUTPUT data path (second scan path), and the second I/O pin outputs the outputting data from the OUTPUT data path.

Therefore, it would have been obvious to combine Chennupati with AAPA for the benefit of reducing the number pins or allow additional pins to be used for other purposes (Chennupati, col. 5, ll. 34-37).

20. As per claim 11, AAPA teaches the integrated circuit comprising:

any number of scan paths (Specification, page 1, ll. 4-5)and half the number of I/O pins (Specification, page 3, ll. 14-16) wherein:

AAPA does not teach the integrated circuit comprising:

the same number of I/O pins wherein,

each I/O pin is operable to input scan test data during the test time; and

a tester determines the function of each I/O pin during the test time.

Chennupati teaches a system and a method comprising:

a single bi-directional pin (Fig. 1, ref. 152) is utilized for both inputting and outputting of data (col. 1, ll. 15-17 and col. 4, ll. 23-25); and

an arithmetic unit (Fig. 1, ref. 164) and a driver (Fig. 1, ref. 145) utilized for determining if the interface port (Fig .1, ref. 152) is currently operating as input (as the arithmetic unit compares the signal levels S3 and S4 to determine the INPUT2 signal; col. 4, ll. 61-64), as output (as the driver outputs the OUTPUT2 signal) or as both input and output (as OUTPUT1 signal is detected and received by the arithmetic unit, and at the same time, the driver outputs the OUTPUT2 signal; col. 5, ll. 15-25).

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to include Chennupati's bi-directional pin, the arithmetic unit and the driver into AAPA's I/O pins. The resulting combination of the references teaches the integrated circuit further comprising wherein the number of I/O pins is the same as the number of scan path, as each I/O pins can operate as both input and output, therefore each I/O pins is operable to input data during a period of time, wherein the period of time is utilized for determining if the I/O pin is currently operating as input pin, as output pin or simultaneously as input and output pin.

Therefore, it would have been obvious to combine Chennupati with AAPA for the benefit of reducing the number pins or allow additional pins to be used for other purposes (Chennupati, col. 5, ll. 34-37).

21. As per claim 12, AAPA teaches an integrated circuit comprising:

a functional circuit (Drawings, Fig. 1, ref. 5) operable to produce functional output (Specification, page 1, ll. 25-31);

a scan path (Drawings, Fig. 1, ref. 9) operable to produce scan output (Specification, page 1, ll. 8-9);

a first I/O pin (Drawings, Fig. 1, ref. 2) operable to be used as input at a first time (Specification, page 1, ll. 5-8);

a second I/O pin (Drawings, Fig. 1, ref. 12) operable to be used as output at a second time (Specification, page 1, ll. 5-8);

a flip-flip (Drawings, D flip-flop 20 of Fig. 1) coupled to the input of the initial seed value (Drawings, Fig. 4, ref. 21) and the output of the scan input data (Drawings, Fig. 4, ref. 21) (Specification, page 2, ll. 30-32) and operable to hold the functional output or the scan output for a clock cycle (Drawings, Fig. 4 and Specification, page 3, ll. 1-3), as the scan output data (Drawings, Fig. 4, ref. 28) is outputted to the D flip-flop and it is well know that the D flip-flop can hold data for a clock cycle; and

utilizing the flip flop for the purpose of reseeding (Specification, page 2, ll. 27-33).

AAPA does not teach the integrated circuit comprising a I/O pin operable to be used as input at a first time and as output at a second time, and further more, does not expressly teach that the flip-flop is coupled to the I/O pin and to the functional circuit and the scan path.

Chennupati teaches a system and a method comprising a single bi-directional pin (Fig. 1, ref. 152) is utilized for both inputting and outputting of data (col. 1, ll. 15-17 and col. 4, ll. 23-25) and the data is inputted into a device (Fig. 2, ref. 150) through a INPUT2 data path and outputted from the device through the OUTPUT2 data path (Fig. 1, ref. 156), wherein the received INPUT2 data would have been processed by other components in the device to generated the OUTPUT2 data to be outputted (Fig. 1 and col. 4, ll. 27-29).

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to include Chennupati's bi-directional pin into AAPA's first and second I/O pins.

The resulting combination of the references teaches the integrated circuit further comprising the first and second I/O pin is operable to input scan data at the first time and to output scan data at the second time, and further more, it would have been obvious that the D flip-flop is coupled to the I/O pin to obtain the initial seed value, and coupled to the scan path for inputting the scan input data, and coupled to the functional circuit (components in the device) as the scan input data would be processed by the components before outputting, therefore, implementing the reseeding and provide a more complex self-generating test (AAPA, Specification, page 3, ll. 1-3).

Therefore, it would have been obvious to combine Chennupati with AAPA for the benefit of reducing the number pins or allow additional pins to be used for other purposes (Chennupati, col. 5, ll. 34-37).

22. As per claim 13, AAPA and Chennupati teach all the limitation of claim 12 as discussed above, where both further teach the integrated circuit further comprising:

a number of scan paths (Chennupati, Fig. 2 and col. 5, ll. 38-44) as each of the plurality of bus lines have the corresponding scan path resulting in four scan path;

the same number of I/O pads (Chennupati, Fig. 2 and col. 5, ll. 38-44) as there are four I/O pads connected to the corresponding bus line; and

the same number of flip-flops (AAPA, Drawings, Fig. 3, ref. 17 and Fig. 4, ref. 20) operable to form at least one register, as each of the I/O pad is coupled to the D flip-flop, therefore the combined plurality of D flip-flops forms the at least one register.

23. As per claim 14, AAPA and Chennupati teach all the limitation of claim 13 as discussed above, where AAPA further teaches the integrated circuit further comprising:

each I/O pad comprises a scan output buffer (AAPA, Drawings, D flip-flop 17 of Fig. 3), as the scan output data is buffered in the D flip-flop before being outputted;

each flip flop (AAPA, Drawings, D flip-flop 17 of Fig. 3) comprising:

a compact-control signal (AAPA, Drawings, mask signal 13 of Fig. 3);

an output-data signal (AAPA, Drawings, scan output data (SOD) 8 of Fig. 3); and

an AND-gate (AAPA, Drawings, Fig. 3, ref. 15) operable to eliminate don't-care data (AAPA, Specification, page 2, ll. 20-25), as the AND-gate is utilized to eliminate the output of data with don't-care nature; and

the register is operable as a compaction register (AAPA, Drawings, Fig. 2, and Specification, page 2, ll. 1-5), as each of the I/O pads is operable for both inputting scan input data (SID) and outputting scan output data (SOD), therefore it would have been obvious to implement the compactor at the I/O pads for outputting and utilizing the register as compaction register.

24. As per claim 15, AAPA and Chennupati teach all the limitation of claim 13 as discussed above, where AAPA further teaches the integrated circuit comprising wherein each I/O pad further comprises:

a reseed multiplexer (AAPA, Drawings, Fig. 4, ref. 25) operable to receive functional output data (AAPA, Drawings, scan output data 28 of Fig. 4) and scan input data (AAPA, Drawings, Fig. 4, ref. 23);

a reseed control signal operable to control the reseed multiplexer (AAPA, Specification, page 2, l. 31 to page 3, l. 3), wherein the reseed multiplexer is multiplexing input data between the scan input data and the output of the XOR-gate (AAPA, Drawings, Fig. 4, ref. 29), therefore the reseed control signal is required to determine which of the input is to be outputted to the D flip-flop (AAPA, Drawings, Fig. 4, ref. 20); and

the register is operable as a reseed register (AAPA, Specification, page 2, l. 27 to page 3, l. 3) as the register is utilized for reseeding.

25. As per claim 16, AAPA and Chennupati teach all the limitation of claim 15 as discussed above, where AAPA further teaches the integrated circuit comprising wherein:

each I/O pad further comprises an XOR-gate (AAPA, Drawings, Fig. 4, ref. 29) operable to receive input from the output of a linear feedback shift register (AAPA, Drawings, Fig. 4, ref. 27 and Specification, page 3, ll. 1-3); and

the register is operable as a linear feedback shift register (Specification, page 3, ll. 1-3) as the scan output data is feedback to the register.

26. As per claim 17, AAPA and Chennupati teach all the limitation of claim 13 as discussed above, where AAPA further teaches the integrated circuit comprising:

a second number of flip-flops (AAPA, Drawings, Fig. 3, ref. 17) operable to form a compaction register wherein:

the integrated circuit is operable to perform reseeding (AAPA, Specification, page 2, l. 27 to page 3, l. 3), wherein the reseeding is performed by the different number of flip-flops (AAPA, Drawings, Fig. 4, ref. 20); and

the integrated circuit is at the same time operable to perform compaction (AAPA, Specification, page 2, ll. 20-26), wherein compaction is performed by the second number of flip-flops.

27. As per claim 18, AAPA and Chennupati teach all the limitation of claim 17 as discussed above, where AAPA further teaches the integrated circuit comprising wherein

the compaction register can be read serially (AAPA, Specification, page 1, ll. 7-9), as shifting of data is implemented serially.

28. As per claim 19, AAPA teaches a method comprising:

inputting scan data to a first I/O pin (Drawings, Fig. 1, ref. 2) during a first time (Specification, page 1, ll. 5-8);

processing the scan data in a scan path to produce scan output data (Specification, page 1, ll. 8-9); and

outputting the scan output data to a second I/O pin (Drawings, Fig. 1, ref. 12) at a second time (Specification, page 1, ll. 5-8).

AAPA does not teach the method comprising wherein the input and the output of data are transferred over the same I/O pin.

Chennupati teaches a system and a method comprising a single bi-directional pin (Fig. 1, ref. 152) is utilized for both inputting and outputting of data (col. 1, ll. 15-17 and col. 4, ll. 23-25).

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to include Chennupati's bi-directional pin into AAPA's first and second I/O pins. The resulting combination of the references teaches the integrated circuit further comprising the first I/O pin is operable to input scan data during the first time and to output scan data during the second time.

Therefore, it would have been obvious to combine Chennupati with AAPA for the benefit of reducing the number pins or allow additional pins to be used for other purposes (Chennupati, col. 5, ll. 34-37).

29. As per claim 20, AAPA and Chennupati teach all the limitation of claim 19 as discussed above, where AAPA further teaches the method comprising:

multiplexing output data (AAPA, Drawings, Fig. 1, ref. 6) and scan output data (AAPA, Drawings, Fig. 1, ref. 10), wherein output data is outputted by the functional circuit (AAPA, Drawings, Fig. 1, ref. 5); and

storing the output data or scan output data in a flip-flop (AAPA, Drawings, D flip-flop 17 of Fig. 3) during the first time, as data is buffered in the flop-flop before outputting during the second time.

30. As per claim 21, AAPA and Chennupati teach all the limitation of claim 20 as discussed above, where both further teach the method comprising:

connecting a number of flip-flops (AAPA, Drawings, D flip-flop 17 of Fig. 3 and D flip-flop 20 of Fig. 4) associated with I/O pins; and

forming a register (AAPA, Drawings, D flip-flop 20 of Fig. 4) performing a reseed test (AAPA, Specification, page 2, l. 27 to page 3, l. 3 and Chennupati, Fig. 2), wherein there are four I/O pins and each is connected to the corresponding D flip-flop (AAPA, Drawings, Fig. 4, ref. 20) to form the register for implementing reseeding test.

31. As per claim 22, AAPA and Chennupati teach all the limitation of claim 21 as discussed above, where AAPA further teaches the method comprising wherein forming a register further comprises:

sending a compact control signal (AAPA, Drawings, mask signal 13 of Fig. 3);

AND-gating (AAPA, Drawings, AND-gate 15 of Fig. 3) the compact control signal with the output data (AAPA, Drawings, scan output data (SOD) 8 of Fig. 3);

eliminating don't care data (AAPA, Specification, page 2, ll. 14-26), wherein the AND-gate is utilized to eliminate the don't care data; and

performing compaction (AAPA, Drawings, Fig. 2-3).

32. As per claim 23, AAPA and Chennupati teach all the limitation of claim 21 as discussed above, where AAPA further teaches the method comprising wherein forming a register further comprises:

sending a reseed control signal to a reseed multiplexer (AAPA, Drawings, Fig. 4, ref. 25), wherein the reseed multiplexer is multiplexing between two inputs, therefore there must be the corresponding reseed control single controlling the reseed multiplexer to select between the two input signals;

multiplexing functional output data (AAPA, Drawings, Fig. 4, ref. 28) and scan input data (AAPA, Drawings, Fig. 4, ref. 23); and

performing a reseed test (AAPA, Specification, page 2, l. 27 to page 3, l. 3).

33. As per claim 24, and Chennupati teach all the limitation of claim 23 as discussed above, where AAPA further teaches the method comprising wherein multiplexing further comprises:

receiving gated input from a linear feedback shift register (AAPA, Drawings, Fig. 4, ref. 27) as the output from the linear feedback shift register is inputted into the XOR-gate, to be multiplexed by the reseed multiplexer; and

performing a linear feedback shift register reseed test (AAPA, Specification, page 2, l. 27 to page 3, l. 3), as the scan output data is feedback to the register.

34. As per claim 25, AAPA and Chennupati teach all the limitation of claim 19 as discussed above, where Chennupati further teaches the method comprising wherein the first time and the second time occur during the same clock cycle (Chennupati, col. 1, ll. 26-28), as the port can simultaneous transmit and receive input and output signal, therefore the inputting and the outputting of data can be implemented over the same clock cycle.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chun-Kuan (Mike) Lee whose telephone number is (571) 272-0671. The examiner can normally be reached on 8AM to 5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Fritz M. Fleming can be reached on (571) 272-4145. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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